

vtpci_modern_register
_cfg_msix

vtpci_modern_register
_vq_msix

vtpci_modern_register_msix

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graph LR; A[vtpci_modern_register_cfg_msix] --> C[vtpci_modern_register_msix]; B[vtpci_modern_register_vq_msix] --> C;
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The diagram illustrates a mapping or aggregation process. On the left, there are two separate boxes representing source components: 'vtpci_modern_register_cfg_msix' (top) and 'vtpci_modern_register_vq_msix' (bottom). Blue arrows from both boxes point towards a single, larger box on the right labeled 'vtpci_modern_register_msix'. This target box is shaded gray, indicating it is the final or consolidated result of the process.