

dwc\_otg\_host\_data\_rx

dwc\_otg\_host\_data\_tx

dwc\_otg\_host\_rate\_check

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graph LR; A[dwc_otg_host_data_rx] --> C[dwc_otg_host_rate_check]; B[dwc_otg_host_data_tx] --> C;
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The diagram illustrates a data flow where two separate input components, 'dwc\_otg\_host\_data\_rx' and 'dwc\_otg\_host\_data\_tx', both feed into a single processing component, 'dwc\_otg\_host\_rate\_check'. The input boxes are white with black borders, while the output box is shaded gray with a black border. Blue arrows indicate the direction of the flow from left to right.