

collect_edc0_meminfo

collect_edc1_meminfo

collect_mc0_meminfo

collect_mc1_meminfo

cudbg_t4_fwcache

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graph LR; A[collect_edc0_meminfo] --> D[cudbg_t4_fwcache]; B[collect_edc1_meminfo] --> D; C[collect_mc0_meminfo] --> D; E[collect_mc1_meminfo] --> D;
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The diagram illustrates a data flow where four separate memory information collection processes (collect_edc0_meminfo, collect_edc1_meminfo, collect_mc0_meminfo, and collect_mc1_meminfo) all feed into a single target component (cudbg_t4_fwcache). Each source box is connected to the target box by a blue arrow pointing towards the right.