



Video Electronics Standards Association

VESA

VBE/SCI™ Standard

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VESA BIOS Extension/Serial Control Interface Standard

Version: 1.0

Revision: 2

Date: July 2, 1997

Purpose

To establish a standard set of low level, hardware-independent system services for reading and writing information via the I²C™ serial interface.

Summary

These low level functions provide a hardware abstraction layer for reading and writing serial data via the I²C serial interface, enabling higher level interfaces such as DDC and future hardware standards to be layered on top of existing controllers without having to update the internal BIOS and driver interface functionality.

These functions supplement the VESA BIOS Extensions (VBE) normally provided in ROM with the display controller and accessed through interrupt 10h. These functions also supplement the VESA BIOS Extensions/Accelerator Functions (VBE/AF) via the Supplemental Extensions entry point in the 32-bit loadable driver.

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Any industry standard requires input from many sources. This document was made possible by the joint efforts of the members of the VESA Monitor Committee and the VESA Software Standards Committee during 1993, 1994 and 1997. In particular, the following individuals and their companies contributed with time and knowledge.

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Kendall Bennett, SciTech Software, Inc.
Tom Ryan, SciTech Software, Inc.
Sebastien Marsanne, SGS Thomson.
Bill Milford, STB Systems.

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This document contains the VESA BIOS Extension, Serial Control Interface (VBE/SCI) specification for standard software access to the I²C serial interface between the display controller and the display device without specific hardware knowledge or direct hardware access. It is intended for use by system software developers developing hardware devices or operating systems. This document describes the interface extensions to the VBE/Core Video BIOS software interrupt mechanism (Int 10h), but it is equally applicable to the VBE/AF Accelerator Functions 32-bit loadable driver specification (via the Supplemental Extensions function provided by the VBE/AF 2.0 and later specifications).

Readers of this document should already be familiar with the VESA Video BIOS extensions and programming video hardware at the BIOS level. The VESA BIOS Extensions are defined by the VESA VBE/Core specification available from the VESA office. The VESA BIOS Extensions/Accelerator Functions are defined by the VESA VBE/AF specification also available from the VESA office.

Scope of the VBE/SCI Standard

The VESA BIOS Extension/Serial Control Interface (VBE/SCI) provides a hardware-independent means for operating system and configuration utility software to read and write data over the I²C serial control interface. The I²C interface forms the backbone of the DDC Hardware standard for communication between the display controller and any attached display devices. Although the VBE/DDC interface exists for reading EDID information blocks from the display device, this hardware standard can be used to implement the DDC protocol in a hardware-independent fashion. More importantly, these low level functions can be used to implement future higher level protocols for one-way and two-way communication between the display controller and the attached display device without the need to update or revise the BIOS or hardware drivers for a particular piece of display controller hardware.

The VBE/SCI services should be provided as part of the Video BIOS ROM since the functions may need to be used during system bootup. The VBE/SCI services may also be provided as part of a VESA VBE/AF 32-bit loadable driver, which can be used by the operating system at bootup time, or at runtime to talk to the attached display device.

The VBE/SCI services can be implemented with a standard VGA BIOS, and do not require the support of other VESA VBE BIOS services.

This chapter describes in detail each of the functions defined by the VBE/SCI standard. The extended BIOS calls have been defined to map into a standard VGA BIOS, as well as all implementations of a VESA VBE/Core BIOS. It is also designed to coexist with (and eventually replace) the VBE/DDC software interface standard. In order to maintain compatibility with these environments, the VBE/SCI function calls are grouped under the VBE function number 4Fh, sub-function 15h (VBE/DDC sub-function). The number 4F15h is passed in the AX register to the INT 10h software interrupt handler.

These functions are also callable via the VESA VBE/AF Accelerator Functions standard (VBE/AF 2.0 and later) through the Supplemental Extensions entry point. Application software wishing to call the VBE/SCI functions via VBE/AF will load the machine registers as required for a regular INT 10h software interrupt, but will make call the Supplemental Extensions entry point instead of issuing and INT 10h software interrupt.

VBE/SCI Return Status

The AX register is used to indicate the completion status upon return from VBE/SCI functions. If VBE/SCI support for the specified function is available, the 4Fh value passed in the AH register on entry is returned in the AL register. If the VBE/SCI function completed successfully, 00h is returned in the AH register. Otherwise, the AH register is set to indicate the nature of the failure.

VBE RETURN STATUS

AL == 4Fh:	Function is supported
AL != 4Fh:	Function is not supported
AH == 00h:	Function call successful
AH == 01h:	Function call failed

Note: Applications should treat any non-zero value in the AH register as a general failure condition as later versions of VBE/SCI may define additional error codes.

Function 15h, Sub-function 10h - Report VBE/SCI Capabilities

Input:	AX	= 4F15h	VBE/SCI Interface Extensions
	BL	= 10h	Report VBE/SCI Capabilities
Output:	AX	=	VBE Return Status
	BL	=	I2C level supported
			bit 0 - Can write to SCL clock line
			bit 1 - Can write to SDA data line
			bit 2 - Can read from SCL clock line
			bit 3 - Can read from SDA data line
	CX	=	VBE/SCI version number.
	DX	=	Maximum number of monitor ports supported.

Note: All other registers are preserved.

This function returns the capabilities of the VBE/SCI BIOS interface along with the revision level of the VBE/SCI implementation. The BL register contains the hardware I²C capabilities for the display controller. Where a bit is 0, the feature is not supported and where a bit is 1, the feature is supported. Hence if bit 2 is set to 0, then support for writing to the SCL clock line is not provided by the display controller.

The CX register contains a BCD value, which specifies the software revision level of the VBE/SCI interface. The higher byte specifies the major version number. The lower byte specifies the minor version number. The BCD value for VBE/SCI 2.0 is 0200h and the BCD value for VBE/SCI 2.1 would be 0201h.

The DX register contains the maximum number of monitor ports supported by the graphics controllers. A value of 0 indicates the primary monitor port and subsequent ports are assigned 01, 02, etc (no gap in used port number is allowed) up to the maximum number of monitor ports supported. In systems with integral monitors, port 0 should be the port connected to the primary internal monitor. Note that this is only intended to support controllers that have multiple independent outputs on a single card (i.e.: a controller with a VGA/EVC connector and a TVOut connector that can display simultaneously). Support for two independent controllers in a single system is provided via the VBE/AF 2.0 and later specification, which includes support for multiple independent controllers.

Note: It is up to the application developer to check the capabilities of the underlying hardware to determine if it can support the high level protocols that the application wishes to use (i.e.: if you require writing to the SCL clock line and the hardware does not support this, the application will have to handle this appropriately).

Note: Hardware vendors building new hardware devices should include support for reading and writing to both the SCL and SDA lines for maximum compatibility with this standard and all future standards based on the serial control interface.

Function 15h, Sub-function 11h - Begin SCL/SDA control

Input:	AX	= 4F15h	VBE/SCI Interface Extensions
	BL	= 11h	Begin SCL/SDA control
	CX	=	Monitor port number
Output:	AX	=	VBE Return Status

Note: All other registers are preserved.

This function enables support for reading and writing the SCL/SDA control lines for the graphics controller, and *must* be called before sub-functions 14-16 are called to read and write values to the SCL/SDA control lines. This function allows the graphics controller to do any necessary re-programming of the hardware to enable the I²C interface to make sure that the read/write functions can be executed as efficiently as possible (and also to arbitrate between multiple monitor ports).

CX is passed a value that represents the monitor port number that should be used to enable SCL/SDA control for, and this same value must be passed to all subsequent calls to sub-functions 14-16. Note that only one monitor port may be active for SCL/SDA control at a time, so you should not call begin for monitor port 0 and then call begin for monitor port 1 without first calling end for monitor port 0.

Note: It is up to the application programmer to ensure that the begin/end SCL/SDA control functions are called before sub-functions 14-16h are called, and the behavior of the BIOS if this is not done is undefined.

Function 15h, Sub-function 12h - End SCL/SDA control

Input:	AX	= 4F15h	VBE/SCI Interface Extensions
	BL	= 12h	End SCL/SDA control
	CX	=	Monitor port number
Output:	AX	=	VBE Return Status

Note: All other registers are preserved.

This function disables support for reading and writing the SCL/SDA control lines for the graphics controller, and *must* be called after sub-functions 14-16h are called to read and write values to the SCL/SDA control lines.

CX is passed a value that represents the monitor port number that should be used to disable SCL/SDA control for, and must be the same value passed to the begin function.

Function 15h, Sub-function 13h - Write SCL clock line

Input:	AX	= 4F15h	VBE/SCI Interface Extensions
	BL	= 13h	Write SCL clock line
	CX	=	Monitor port number
	DX	=	Binary value to write to clock line (0 or 1)
Output:	AX	=	VBE Return Status

Note: All other registers are preserved.

This function sets the SCL clock line to the specified binary value (0 or 1) passed in the DX register. After this function has been called, the SCL line will remain at the specified value until re-programmed to a new value.

CX is passed a value that represents the monitor port number that should be used, and must be the same value passed to the begin function (sub-function 11h).

Function 15h, Sub-function 14h - Write SDA data line

Input:	AX	= 4F15h	VBE/SCI Interface Extensions
	BL	= 14h	Write SDA data line
	CX	=	Monitor port number
	DX	=	Binary value to write to data line (0 or 1)
Output:	AX	=	VBE Return Status

Note: All other registers are preserved.

This function sets the SDA data line to the specified binary value (0 or 1) passed in the DX register. After this function has been called, the SDA line will remain at the specified value until re-programmed to a new value.

CX is passed a value that represents the monitor port number that should be used, and must be the same value passed to the begin function (sub-function 11h).

Function 15h, Sub-function 15h - Read SCL clock line

Input:	AX	= 4F15h	VBE/SCI Interface Extensions
	BL	= 15h	Read SCL clock line
	CX	=	Monitor port number
Output:	AX	=	VBE Return Status
	DX	=	Binary value read from clock line (0 or 1)

Note: All other registers are preserved.

This function reads the current binary value of the SCL clock line (0 or 1) in the DX register.

CX is passed a value that represents the monitor port number that should be used, and must be the same value passed to the begin function (sub-function 11h).

Function 15h, Sub-function 16h - Read SDA data line

Input:	AX	= 4F15h	VBE/SCI Interface Extensions
	BL	= 16h	Read SDA data line
	CX	=	Monitor port number
Output:	AX	=	VBE Return Status
	DX	=	Binary value read from data line (0 or 1)

Note: All other registers are preserved.

This function reads the current binary value of the SDA data line (0 or 1) in the DX register.

CX is passed a value that represents the monitor port number that should be used, and must be the same value passed to the begin function (sub-function 11h).

Appendix 1 - Related Documents

- VBE/Core Functions Specification
- VBE/AF Accelerator Functions Specification
- VESA DDC Hardware Specification